Shreenanda S

Shivamogga

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Summary

I'm a self-motivated and passionate final year Electronics and Telecommunication student. I have developed good domain related skill set and problem-solving capabilities. My keen technical interests include embedded hardware development, digital circuits design and verification and programming.

Technical Skills

- **Languages**: Verilog HDL, System Verilog, UVM, Embedded C, C/C++, Python.
- **Technologies/Frameworks**: Digital Electronics,8051 microcontroller, RISC-V Processor, Arm Architecture, Linux, Operating Systems.
- **Developer Tools**: MATLAB, SCILAB, PCB Design, PyCharm, Flask, Git, Xilinx Vivado, Open Lane, Yosys, FPGA.
- **Embedded Systems:** Raspberry pi, Arduino Uno, ESP8266, ESP32, GPS, LiDAR.
- **Soft Skills:** Project Management, Quick Learning, Leadership, Teamwork, Independent working.

Education

Jawaharlal Nehru New College of Engineering — **CGPA: 8.20 - Aug 2025**
Bachelor of Engineering in Electronics and Telecommunication — *Shivamogga, Karnataka*

DVS COMP PU College — **77.66% - Jul 2021**
Pre-University, PCMCs — *Shivamogga, Karnataka*

Sahyadri English Medium High School — **74.56% -Apr 2019**
High School, State board — *Shivamogga, Karnataka*

Internships

- **Diploma in VLSI System Design –** Cranes Varsity (6 Months)
- **Cyber Security**-IBM Skills Build (6 weeks)

Certificates

- **Microelectronics: Devices to Circuits** - NPTEL (30/06/2023)
- **Microprocessors and Microcontrollers** - NPTEL (31/12/2023)
- **VLSI design flow: RTL to GDS** - NPTEL (26/10/2024)
- **PCB Design and Testing** - JNNCE (11/03/2023)

Projects

Cyclic Redundancy Check | *Verilog, Xilinx Vivado,FPGA*

- Designed and implemented a CRC encoder and Decoder for error Detection in digital communication Systems.

2-bit Vedic Multiplier | *Verilog, Xilinx Vivado, Yosys*

- Designed and implemented a 2-bit Vedic multiplier using RTL logic in Verilog, based on the Urdhva Tiryagbhyam sutra for high-speed multiplication.
- Performed functional verification using testbenches and synthesized the design on Yosys, ensuring minimal area and delay.

Verilog implementation | *Verilog, Xilinx Vivado*

- Adder, Mux, De-Mux, Encoder, Decoder, FSM, Gray Converter, Magnitude, Comparator, Flip-Flops, Counter's, Memories, CRC, UART, SPI, I2C, ALU.

Swastha Nari: Automatic Sanitary Napkin Vending Machine | *C, Python, Arduino Uno, ESP8266, RFID Reader*

- Developed an automated vending machine for sanitary napkins using UPI payments and RFID card authentication.

Steganography: Secure Text Hiding in Images |*Python*, *PyCharm*

- Designed an image-based steganography system to hide and retrieve text securely.

Smart Attendance System Using Face Recognition | *Python, Fire Base, Raspberry Pi, OpenCV, RFID*

- Developed an attendance system using facial recognition to ensure contactless and accurate identification.

Clever Commute: Autonomous Vehicle for Smart Mobility & Public Safety | *Python, Raspberry Pi, LiDAR, GPS, Camera*

- Designed a self-driving vehicle integrating Raspberry Pi, LiDAR, GPS, and camera module for real-time navigation and decision-making.

Leadership / Extracurricular

SIGMA 2K24 – State-Level Technical Symposium ***2024***
Student Convener *JNNCE*

1st Place, Maze Solver ***2024***
PLASMA2K24 *JNNCE*

1st Place, Robo Rush | 2nd place, Line Follower ***2024***
19th ISTE Karnataka State-level Student Convention *P.E.S,Mandya*

2nd Place, Death Valley ***2024***
Advitiya-24 National Level Students Technical Fest *K.L.E,Hubballi*

2nd Place, Fast N Furious ***2024***
RoboFiesta'24 *RVIT,Banglore*

Participated in Amphibot ***2024***
Conscientia2k24 *IIST,Kerala*

Participated in Project Presentation ***2024***
Janana-Vijnana-Tantrajnana Mela-2024 *mandya*